Claims

[redacted]

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Amendments to the Claims: filed on 11/10/05 by applicant.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claim 63 without prejudice.

Please amend claim 62 as follows:

Claims 1-33 (canceled)

34. (original): A system for generating complex conditions formed by a Boolean combination of relations comprising:

an arithmetic unit which receives at least two operands from a register file;

instruction control lines derived from a registered instruction in a processor pipeline, the instruction control lines including conditional execution control lines to control conditional operation as specified in an instruction;

the arithmetic unit producing a result and a latched arithmetic scalar condition state;

a first latch for holding the arithmetic scalar condition state for the instruction after the instruction has finished its execution state;

a second latch connected to the conditional execution control lines for holding instruction control signals for the instruction after the instruction has finished its execution state;

an arithmetic condition flag (ACF) generation unit for providing a Boolean combination of a present selected state with a previous state; and

an ACF latch for storing the previous state and feeding the previous state back to the ACF generation unit.

35. (original): The system of claim 34 wherein the ACF latch is a programmer visible latch.

36. (original): The system of claim 34 further comprising a multiplexer connected to receive said Boolean combination from the ACF generation unit and to controllably switch said Boolean combination or said AFC latch to branch logic in a sequence processor (SP).

37. (original): The system of claim 34 further comprising an arithmetic scalar flag (ASF) latch switchably connected to the said first latch arithmetic scalar condition state output of the arithmetic unit.

38. (original): The system of claim 37 wherein the switchable connection of the said first latch arithmetic scalar condition state output of the arithmetic unit and the ASF latch comprises a controllable multiplexer.

39. (original): The system of claim 38 wherein an output of the controllable multiplexer controllably switches the arithmetic scalar condition state or the ASF latch output to the branch logic in a sequence processor (SP).

40. (original): The system of claim 37 wherein the ASF latch is a programmer visible latch.

Claims 41-52 (canceled)

53. (original): A system for generating complex conditions comprising:

an arithmetic unit which receives at least two operands from a register file;

instruction control lines derived from a registered instruction in a processor pipeline, the instruction control lines including conditional execution control lines to control conditional operation as specified in an instruction;

the arithmetic unit producing a result and a latched arithmetic scalar condition state;

a first latch for holding the arithmetic scalar condition state for the instruction after the instruction has finished its execution state;

a second latch connected to the conditional execution control lines for holding instruction control signals for the instruction after the instruction has finished its execution state;

an arithmetic condition flag (ACF) generation unit for providing a present selected state of a plurality of arithmetic condition flags (ACFs); and

an ACF latch for storing a previous state for the ACFs and feeding the previous state back to the ACF generation unit.

Claims 54 and 55 (canceled)

56. (previously presented): The system of claim 53 wherein the ACF latch is a programmer visible latch.

57. (previously presented): The system of claim 53 further comprising a multiplexer connected to receive said present selected state from the ACF generation unit and to controllably switch said Boolean combination or said AFC latch to branch logic in a sequence processor (SP).

58. (previously presented): The system of claim 53 further comprising an arithmetic scalar flag (ASF) latch switchably connected to the first latch arithmetic scalar condition state output of the arithmetic unit.

59. (previously presented): The system of claim 58 wherein the switchable connection of the first latch arithmetic scalar condition state output of the arithmetic unit and the ASF latch comprises a controllable multiplexer.

60. (previously presented): The system of claim 59 wherein an output of the controllable multiplexer controllably switches the arithmetic scalar condition state or the ASF latch output to the branch logic in a sequence processor (SP).

61. (previously presented): The system of claim 58 wherein the ASF latch is a programmer visible latch.

62. (currently amended): A processing system comprising:

an arithmetic unit receiving at least two operands from a register file, performing an operation on the at least two operands, and producing a result and an arithmetic scalar condition state;

conditional execution control signals derived from an instruction in an instruction pipeline to control conditional operation as specified in the instruction; ~~and~~

an arithmetic condition flag (ACF) generation unit for receiving both the conditional execution control signals and the arithmetic scalar condition state, and for providing a present selected state of a plurality of arithmetic condition flags (ACFs); and

a storage unit for storing a previous state of the ACFs and for feeding the previous state back to the ACF generation unit.

63. (cancelled)

64. (previously presented): The system of claim 62 wherein the arithmetic scalar condition state includes at least one of a carry flag, an overflow flag, a sign flag and a zero flag.

65. (previously presented): The system of claim 62 wherein said instruction is a compare instruction.

66. (previously presented): The system of claim 62 further comprising a sequence processor including instruction branch control logic, wherein the ACFs are provided to the branch control logic.